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## Gabriele Gorla <gorlik@yahoo.com>

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1031 Clyde Ave #504

Santa Clara, CA 95054

### OBJECTIVE

Leadership position in product or system design in a growing company. Enjoy fast paced environment, travel and customer or vendor contact. Willing to relocate.

### SKILLS

System architecture, project planning and execution, high speed PCB design, PCB and ASIC bring up and debugging, Design for Cost, Design for Manufacturing, technical writing, multiphase DC-DC converters, DDR1/2/3, GDDR3/GDDR5, PCIe, DisplayPort, PCI, AGP, TMDS/HDMI, LVDS, USB, C, C++, Linux, MacOS, OpenGL, 8-b and 32-b microcontrollers, spice, LaTeX.

### WORK EXPERIENCE

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#### **NVIDIA Corp., Santa Clara, CA**

*2011-present*

##### **Sr. Engineering Manager, Product Design Engineering**

- Manage a team of 30 hardware design and validation engineers in US and Asia
- Lead multi discipline team including mechanical, thermal, RF and industrial design
- Responsible for entire product lifecycle including definition, design, validation, NPI, manufacturing and RMA for several product lines: Quadro (Workstation), Tesla (High Performance Computing), Grid (cloud computing), entry level GeForce (consumer) and selected Tegra based products
- Managed architecture, design, validation and NPI of the Tegra based NVIDIA Shield portable gaming console
- Manage relationship with all critical components vendors
- Support sales and marketing teams on both pre and post sales activities
- Support manufacturing team during ramp and production
- Lead DC-DC conversion efficiency initiative to improve performance/watt in high performance computing environments
- Managed the design of the NVIDIA K20x SXM module for the Cray TITAN supercomputer (Oak Ridge National Lab)
- Managed the re-design of Quadro 600, Quadro 2000, Quadro 4000 and Quadro 5000

#### **NVIDIA Corp., Santa Clara, CA**

*2009-2010*

##### **Sr. System Architect, GPU Desktop Engineering**

- Managed design of several desktop PCI-e add-in cards for different market segments (GeForce 8400GS, GT 120, 210, GTX 460, GT 545, GTX 560)
- Led the Design for Cost initiative to reduce BOM cost while maintaining or improving the quality of the end product
- Negotiated manufacturing and suppliers requirement with customers
- Supported CEM partners during validation, initial ramp and volume production
- Developed standards to allow re-use of PCB stackups and critical components across several projects to help supply chain management
- Developed processes to avoid single source components on all high volume designs
- Managed technical relationship with vendors for all critical components
- Led system level development of next generation high end GPU including package design, PCB stackup, power delivery, power conversion and signal integrity

#### **NVIDIA Corp., Santa Clara, CA**

*2007-2008*

##### **System Architect, GPU Notebook Engineering**

- Led development of the MXM version 3.0 industry standard specification (<http://www.mxm-sig.org>)
- Managed the design teams for all first generation MXM version 3.0 modules (9600M GT, 9800M GS, 9800M GTX)
- Negotiated with customers and competitors features/requirements for both module and system
- Developed relationship with vendors to establish a component ecosystem to support the specification
- Negotiated design rules with SI team to better fit to low cost, high volume manufacturing

**NVIDIA Corp., Santa Clara, CA**

2005-2007

**Sr. System Design Engineer, GPU Notebook Engineering**

- Led notebook GPU system engineering team
- Main author of notebook GPU design guide, memory performance tuning and several application notes
- Ultimate escalation for customer support, resolved several release critical issues for tier 1 customers
- Hardware support lead for the entire Lenovo discrete graphics notebook line (R61, T61 and T61p)
- Frequent travel to Asia to improve customer relationship, train local employees and resolve critical bugs
- Supported internal engineering for notebook GPUs issues from pre tape-out to production
- Worked with memory vendors to resolve issues and provide support during validation

**NVIDIA Corp., Santa Clara, CA**

2003-2004

**Sr. Applications Engineer, Notebook GPU**

- Led Bringup and characterization team for notebook version of GeForce FX 5600, 6200, 6600 and 7200
- Mentored AEs in difficult customer support issues, train FAE and customers in US and overseas
- Supported marketing/sales in aggressive board and chip sampling schedules
- Designed GeForce FX 5200/5600 (AGP), GeForce PCX and 7200 (PCI-e) notebook reference boards
- Developed models for GPU power dissipation and performance/watt estimation adopted by the entire company
- Designed thermal control system to improve high temperature characterization of notebook chips
- Developed software for cycle accurate DDR1/2 and GDDR3 timing characterization and debug

**NVIDIA Corp., Santa Clara, CA**

2001-2002

**Applications Engineer, Notebook GPU**

- Supported integration of NVIDIA GPUs on customers' platforms during the entire design cycle
- Performed schematics and layout reviews, drove issues to closure in a timely manner
- Supported Apple, Lenovo, HP, Acer and Dell directly and through ODM
- Team member for bringup and characterization of GeForce 2 Go and GeForce 4 Go
- Developed software for signal integrity measurements and statistical analysis of clock jitter

**EDUCATION**

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**University of Minnesota**

1999-2001

**Electrical Engineering**

- Teaching and research assistantship

**The Cooper Union**

1997-1999

**B.E. in Electrical Engineering**

- Full tuition scholarship. Dean's list.

**LANGUAGES**

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Bilingual English/Italian, beginner Mandarin Chinese